

Docket No. 303.703US1
WD # 454509

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CONTACT STRUCTURE
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Serial No.: 09/653,640

Claims 19-36 and 94-102, as of September 25, 2002 (Date of Response to First Office Action).

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19. (Amended) An integrated circuit comprising:
a first device;
a second device;
a contact coupling the first device to the second device; and
a barrier structure encircling the contact.
20. The integrated circuit of claim 19, wherein the first device is a capacitor.
21. The integrated circuit of claim 19, wherein the second device is a transistor.

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22. (Amended) An integrated circuit comprising:
a first device;
a second device;
one or more layers coupling the first device to the second device, at least one of the one or more layers is capable of blocking oxygen atom migration; and
a structure encircling the one or more layers.

23. The integrated circuit of claim 22, wherein the first device is a capacitor.
24. The integrated circuit device of claim 22, wherein the second device is a MOSFET.

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25. An integrated circuit comprising:
a first device;
a second device;
one or more layers coupling the first device to the second device, at least one of the one or more layers is capable of blocking silicon atom diffusion; and
a structure encircling at least two of the one or more layers.
26. The integrated circuit of claim 25, wherein the one or more layers is three.
27. The integrated circuit of claim 25, wherein the structure is fabricated from an oxide.
28. An integrated circuit comprising:
a first device;
a second device;
a multilayer contact including ruthenium silicide, the multilayer contact coupling the first device to the second device; and
an oxide ring encircling the ruthenium silicide.
29. The integrated circuit of claim 28, wherein the multilayer contact includes a polysilicon layer.
30. The integrated circuit of claim 29, wherein the polysilicon layer is separated from the oxide ring by an air gap.
31. An integrated circuit comprising:
a first device;
a second device;

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one or more layers coupling the first device to the second device, at least one of the one or more layers is capable of blocking oxygen atom migration; and
an oxide ring structure encircling at least two of the one or more layers.

32. The integrated circuit of claim 31, wherein at least one of the one or more layers is fabricated from a tungsten nitride.

33. The integrated circuit of claim 32, wherein the oxide ring structure is in contact with the tungsten nitride.

34. An integrated circuit comprising:
a first device;
a second device;
one or more layers electrically coupling the first device to the second device, at least one of the one or more layers is capable of blocking the diffusion of silicon; and
an oxide ring structure encircling at least one of the one or more layers.

35. The integrated circuit of claim 34, wherein at least one of the one or more layers is ruthenium silicide.

36. The integrated circuit of claim 34, wherein the second device is an active device.

94. (Amended) An integrated circuit comprising:
a first device;
a second device;
a contact coupling the first device to the second device; and
a barrier structure of silicon nitride encircling the contact.

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95. The integrated circuit of claim 94, wherein the first device is a capacitor.
96. The integrated circuit of claim 94, wherein the second device is a transistor.
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C4 } 97. (Amended) An integrated circuit comprising:
a first device;
a second device;
one or more layers coupling the first device to the second device, at least one of the one
or more layers including platinum-iridium; and
a structure encircling the one or more layers.
98. The integrated circuit of claim 97, wherein one of the one or more layers comprises a
layer of tungsten nitride having a thickness of between about 900 angstroms and 1100 angstroms.
99. The integrated circuit device of claim 97, wherein the second device is a bipolar
transistor.
100. An integrated circuit comprising:
a first device;
a second device;
one or more layers coupling the first device to the second device, at least one of the one
or more layers including platinum-rhodium; and
a structure encircling at least two of the one or more layers.
101. The integrated circuit of claim 100, wherein the one or more layers includes a polysilicon
layer.

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102. The integrated circuit of claim 100, wherein the first device is formed in a substrate, the substrate selected from a group consisting of silicon, germanium, gallium-arsenide, and silicon-on-sapphire.